REMARKS/ARGUMENTS

Claim rejections 35 U.S.C. § 101

Claims 6, 9-12, 14 and 17-20 are rejected, under 35 U.S.C. §101, because the claimed invention is allegedly directed to non-statutory subject matter. The Applicant respectfully traverses in view of the following.

Independent Claim 6 recites detecting an I/O read instruction, computing a conditional jump address and determining whether to proceed with instruction execution at a next consecutive address or at the conditional jump address, as claimed. As such, embodiments of the present invention determine program flow relating to the claimed conditional jump.

The recited limitation produces a useful result. In order for a microcontroller to properly operate, the address for the next instruction to be executed is required (e.g., next consecutive address or a conditional jump address). Therefore, determining whether to proceed with instruction execution at a next consecutive address or at the conditional jump address, as claimed is useful in that program flow is much more effective.

The recited limitation produces a concrete result e.g., the program flow of the microcontroller is altered based on the claimed determination. The result is

concrete if the process substantially produces the same result again (see *In re Swartz*, 232 F.3d 862, 864, 56 USPQ2d 1703, 1704 (Fed. Cir. 2000) and see MPEP 2100-12). If the in-circuit emulation system executes the same instruction then the result of determining how to proceed with instruction execution, as claimed is the same as before because the same procedure is used in order to determine how to proceed. Accordingly, the recited limitation produces a <u>concrete</u> result.

The recited limitation produces a <u>tangible</u> result because an <u>in-circuit emulation system</u>, which is tangible, performs a serious of steps for branch prediction in order to determine how the in-circuit emulation system should proceed. Accordingly, determining how the in-circuit emulation system should proceed results in a tangible result because the in-circuit emulation system can proceed accordingly or the result of the determination can be stored for later retrieval. Accordingly, the recited limitation produces a <u>tangible</u> result of the program flow is much more efficient due to branch prediction.

Accordingly, independent Claim 6 is directed to statutory subject matter, under 35 U.S.C. §101. Independent Claim 14 recites limitations similar to that of independent Claim 6 and is similarly directed to statutory subject matter for similar reasons. Dependent claims are directed to statutory subject matter by virtue of their dependency.

Claim 13 is rejected, under 35 U.S.C. §101, because the claimed invention is allegedly directed to non-statutory subject matter. The rejection asserts that Claim 13 defines descriptive material and is therefore non-statutory. Moreover, the rejection asserts that Claim 13 depends from "the method according to claim 6," and therefore cannot be properly interpreted as an apparatus claim. The Applicant respectfully traverses in view of the following.

Claim 6 recites an in-circuit emulation system having a virtual microcontroller processing a method of handling conditional jumps, as claimed. Accordingly, Claim 6 recites a virtual microcontroller, which is an apparatus, with process steps. An apparatus with process step is an apparatus claim including functional limitations (see *R.A.C.C. Indus. v. Stun-Tech, Inc.*, 178 F.3d 1309 (Fed. Cir. 1998)). Therefore, the Examiner is misguided in interpreting Claim 6 as a method claim. As such, Claim 13 is also an apparatus claim by virtue of its dependency. The rejection states that an apparatus with descriptive material is statutory according to MPEP 2106. Therefore, Claim 13 is statutory and withdrawal of the rejection is earnestly solicited.

Claim rejections 35 U.S.C. § 112

Claim 13 is rejected under 35 U.S.C. §112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The Applicant respectfully traverses.

Claim 13 has been amended and recites the in-circuit emulation system, wherein instructions are stored in an electronic storage medium for execution as program steps on a programmed processor, as claimed. The Applicant respectfully asserts that in light of the arguments presented above and in light of the amendment, Claim 13 particularly points out and distinctly claims the subject matter of the present invention. As such, withdrawal of the rejection is earnestly solicited.

<u>Claim rejections 35 U.S.C. § 103</u>

Claims 1-4, 6-11 and 13-19 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over U.S. Pat. No. 6,366,878 (hereinafter, Grunert) in view of "Structured Computer Organization, Fourth Edition" by Andres S. Tanenbaum with contribution by James R. Goodman (hereinafter, Tanenbaum). The Applicant respectfully traverses in view of the following.

Independent Claim 1 recites a limitation whereby a virtual microcontroller and a microcontroller execute instructions in lock-step by <u>executing the same instructions using the same clocking signals</u>, as claimed. Moreover, independent

Claim 1 recites a limitation whereby the microcontroller sends I/O read data to the virtual microcontroller, as claimed.

Grunert discloses that the master microcontroller connected to the external memory feeds the memory address (see Grunert, col. 4, lines 41-44). The external memory feeds the data D to the master and the slave microcontroller (see Grunert, col. 4, lines 46-53). Accordingly to Grunert, the external memory feeds the data D to the slave microcontroller whereas independent Claim 1 recites a limitation whereby the microcontroller sends I/O read data to the virtual microcontroller, as claimed.

The Examiner asserts that "the microcontroller initiates a process" and "therefore the master microcontroller sends I/O read data to the virtual microcontroller." However, it is not the microcontroller sending I/O read data to the virtual microcontroller, as claimed but it is the external memory that sends the external data to the slave as discussed above. Initiating a process differs from actual execution of the process, hence sending I/O read data, as claimed. Therefore, the Examiner is misguided in concluding that Grunert teaches the recited limitation because it is not the microcontroller but rather the external memory that is feeding data D to the slave microcontroller.

Moreover, Grunert discloses that the data D read out from the external memory and fed to the master and slave (see Grunert, col. 4, lines 29-53) where the master processes the operating program by evaluating the data from the application system (see Grunert, col. 5, lines 1-2). Grunert discloses that feeding the operating program to the slave serves the purpose of properly timing the control of the data input and output via the ports (see Grunert, col. 5, lines 3-5). Moreover, Grunert discloses that a clock system ensures good synchronization between master and slave (see Grunert, col. 5, lines 8-9).

Accordingly, Grunert discloses that feeding the operating program to the slave controls the timing of input/output data and that the clock ensures a good synchronization between the master and the slave. The Examiner is <u>misguided</u> in concluding that because data transmission between the master and the slave is synchronized and because the master and the slave receive the data D read out from external memory, virtual microcontroller and a microcontroller<u> execute the same instructions using the same clocking signals</u>, as claimed.

The Applicant respectfully reiterates that the mere fact that data transmission is synchronized and that data D read out from external memory is received by both the master and the slave microcontroller <u>does not necessarily translate to</u> or teach execution of the same instructions using the same clocking signal by the microcontroller and the virtual microcontroller, as claimed. For

example, as discussed in the previous response, the data D read out may be fed to both master and slave with good synchronization between the two microcontrollers, however, processing of data D read out by the slave may be significantly after processing of data D read out by the master.

In response to the Applicant's argument, the rejection asserts that "it is unclear where support for this conclusion is found in the reference." In support of the assertion, the Applicant respectfully directs the Examiner's attention to IEEE 100 "THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS," seventh edition, that defines synchronization as "a means of ensuring that both transmitting and receiving stations are operating together in a fixed phase relationship." Therefore, synchronization does not require that the microcontroller and the virtual microcontroller execute the same instruction using the same clock signals, as claimed. As such, synchronization between the master and the slave microcontroller means that they are in fixed phase relationship and does not necessarily mean that the master and the slave execute the same instruction using the same clocking signals.

The rejection admits that Grunert fails to disclose the limitations regarding "means for detecting an I/O read instruction followed by a conditional jump instruction, and for computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with the

microcontroller," as claimed. Moreover, the rejection admits that Grunert fails to disclose the limitation regarding "means for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution at a next consecutive address at the conditional jump address," as claimed. The rejection relies on Tanenbaum to show these limitations. The Applicant respectfully traverses in view of the following.

Tanenbaum discloses that most machines, when they hit a conditional branch, predict whether the branch is going to be taken or not and if a branch is correctly predicted then execution continues at the target address (see Tanenbaum, page 272). Furthermore, the rejection states that the "Applicant's argument appears to force the Tanenbaum reference into the awkward position of contradicting the industry standard terminology as used and known in the art." The rejection further relies on Microsoft Computer Dictionary, Fifth Edition. Assuming *arguendo* that Tanenbaum is in accord with the definition highlighted by Microsoft, Tanenbaum still fails to teach or suggest the recited limitations of Claim 1.

Tanenbaum discloses that "early pipelined machines just <u>stalled</u> until it was known whether the branch would be taken or not" and that stalling "wreaks havoc with the performance" (see Tanenbaum, page 272). Accordingly, Tanenbaum discloses predicting whether to take a branch or not in order to

improve the performance (see Tanenbaum, page 272). Tanenbaum fails to explicitly teach or suggest a virtual microcontroller computing a conditional jump address to remain in lockstep execution with the microcontroller, as claimed.

The rejection states that Tanenbaum teaches a means for keeping the microcontroller in lockstep, as claimed, "specifically branch prediction." The Applicant respectfully traverses in view of the following. The Applicant respectfully reminds the Examiner that Tanenbaum is directed to a computer pipelining (see Tanenbaum, pages 270-272). As discussed above Tanenbaum teaches a method to improve the performance of a computer. The Applicant does not understand Tanenbaum to teach or suggest a virtual microcontroller computing a conditional jump to remain in lockstep execution with the microcontroller, as claimed. Furthermore, the Applicant does not understand the underlying logic for the Examiner's conclusion that "specifically branch prediction" teaches a virtual microcontroller computing a conditional jump to remain in lockstep execution with the microcontroller, as claimed.

Moreover, in response to Applicant's argument the rejection asserts that the microcontroller executing an I/O read instruction followed by a conditional jump instruction, as claimed is taught by Grunert. The Applicant respectfully disagrees in view of the following. As discussed above, Grunert discloses that the data D read out from the external memory is fed to the master and the slave

microcontroller (see Grunert, col. 4, lines 46-47 and 52-53). However, Grunert fails to explicitly teach or suggest executing an I/O read instruction followed by a conditional jump instruction, as claimed. Therefore, the Applicant respectfully requests that the Examiner point to a specific column and line number showing the alleged recited limitation if the rejection is maintained or kindly withdraw the rejection.

Accordingly, the Grunert alone or in combination with Tanenbaum fails to render independent Claim 1 obvious, under 35 U.S.C. §103(a). Independent Claims 6 and 14 are similar in scope to that of independent Claim 1 and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

As per Claim 2, the rejection states that the recited limitation of Claim 2 is an implicit limitation of Claim 1. The Applicant respectfully traverses in view of the following. Independent Claim 1 recites computing a conditional jump address prior to receipt of the conditional jump instruction, as claimed. In contrast, Claim 2 recites a limitation whereby the conditional jump address is computed while the I/O read data are sent from the microcontroller to the virtual microcontroller, as claimed. Accordingly, Claim 2 is not an implicit limitation of Claim 1 because computing a conditional jump before receiving it does not necessarily mean that the conditional jump is computed while the I/O read data are read. Therefore, the

Applicant respectfully submits that the rejection fails to establish a prima facie case of obviousness. Claims 9 and 17 recite a limitation similar to that of Claim 2 and are patentable for similar reasons.

As per Claims 7 and 8, the rejection states that the recited limitations are <u>implicit</u> in Claim 6. The Applicant respectfully disagrees in view of the following. Claim 6 recites a limitation whereby it is determined whether a conditional jump condition is met, as claimed. In contrast, Claim 7 recites executing a next consecutive instruction if the conditional jump condition is not met, as claimed and Claim 8 recites executing an instruction at the conditional jump address in the event the conditional jump condition is met, as claimed. The Applicant respectfully submits that determining whether a conditional jump condition is met <u>does not necessarily</u> translate to executing an instruction at a consecutive instruction or the conditional jump address, as claimed. Accordingly, the Applicant respectfully submits that the rejection has failed to establish a prima facie case of obviousness. Claims 15 and 16 recite a limitation similar to that of Claims 7 and 8 and are patentable for similar reasons.

As such, allowance of Claims 1-4, 6-11 and 13-19 is earnestly solicited.

Claims 5, 12 and 20 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Grunert in view of Tanenbaum and further in view of

U.S. Pat. No. 6,173,419 (hereinafter Barnett). The Applicant respectfully traverses.

The rejection admits that the combination of Grunert and Tanenbaum fails to teach that virtual microcontroller is implemented in a field programmable gate array (FPGA), as claimed. The rejection relies on Barnett to remedy this failure. The Applicant, however, does not understand Barnett to remedy the failures of Grunert and Tanenbaum as discussed above by the Applicant with respect to independent Claim 1. Accordingly, the addition of Barnett to the combination of Grunert and Tanenbaum still fails to teach the limitations of independent Claim 1. Accordingly, the addition Barnett to the cited combination does not render Claims 5, 12 and 20 obvious, under 35 U.S.C. §103(a). As such, allowance of Claims 5, 12 and 20 is earnestly solicited.

Claims 1, 3-5, 6-8, 10-13, 14-16 and 18-20 are rejected under, 35 U.S.C. §103(a) as being allegedly unpatentable over U.S. Pat. No. 6,016,563 (hereinafter Fleisher) in view of Grunert and further in view of "Evaluation of a Branch Target Address Cache" by Sreeram Duvvuru and Siamak Arya (hereinafter Duvvuru). The Applicant respectfully traverses in view of the following.

Fleisher discloses that a programmable logic device, called a mirror device, is essentially identical to the target device (see Fleisher, col. 2, lines 63-65) and operates as an exact replica of the target device in the user-defined target environment (see Fleisher, col. 3, lines 1-2). Accordingly, Fleisher discloses a basic concept of emulation systems. However, Fleisher fails to explicitly teach or suggest a virtual microcontroller executing instructions in lockstep with the microcontroller <u>by executing the same instructions using the same clocking signals</u>, as claimed.

Moreover, Fleisher discloses that a switching module connects input/output pins of the target device and the mirror device (see Fleisher, col. 3, lines 7-12). Fleisher also discloses that in test mode, switches SW2 are closed such that each of the input and bi-directional pins of the target device is coupled via one of switches SW2 to the matching pin of the mirror device (see Fleisher, col. 4, lines 31-35). Fleisher, however, fails to explicitly teach or suggest that the data sent is <u>I/O read data</u>, as claimed.

The rejection states that "the second programmable device has a means for detecting an I/O read instruction followed by a conditional jump instruction [<u>inherent</u> by virtue of executing those instructions]." The Applicant respectfully traverses in view of the following.

The Applicant respectfully submits that the Examiner is misguided in this conclusion because the rejection erroneously presumes that the first programmable device has a mean for detecting an I/O read instruction followed by a conditional jump and therefore the mirror device has a mean for detecting an I/O read instruction followed by a conditional jump. Fleisher fails to teach or suggest that the first programmable device has a mean for detecting an I/O read instruction followed by a conditional jump. Accordingly, the rejection is misguided in concluding that it is inherent by virtue of executing those instructions that the second programmable device has a means for detecting an I/O read instruction followed by a conditional jump instruction.

Moreover, the Applicant respectfully reminds the Examiner that "to establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill" (see MPEP 2100-47). "Inherency, however, may not be established by probabilities or possibilities" and "the mere fact that a certain thing may result from a given set of circumstances is not sufficient" (see In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)).

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination

that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art" (see Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)). As such, the Applicant requests that the Examiner provide sufficient extrinsic evidence to establish the alleged inherency if the rejection is maintained or to kindly withdraw the rejection.

The rejection relies on Grunert to show a system for in-circuit emulation of a microcontroller. Grunert, however, fails to teach or suggest the failures of Fleisher as discussed above by the Applicant.

The rejection admits that the combination of Fleisher and Grunert fails to teach "a virtual microcontroller with means of computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with the microcontroller; and the virtual microcontroller further having means for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution at a next consecutive address or at the conditional jump address." The rejection relies on Duvvuru to remedy these failures. The Applicant respectfully traverses in view of the following.

Duvvuru discloses that the scheme relies on the condition code upon which a branch is based on, and that can be determined slightly ahead of the

branch (see Duvvuru, page 174, right column). Duvvuru further discloses that the BTAC stores branch target addresses, used to start an instruction cache prefetch for expected target instruction flow, the associated condition code bit number together with the branch target address (see Duvvuru, page 174, right column). If the BTAC is hit, the target address and its associated bit are read out and if the specified bit is set in conditional code register (CCR), the target address is cached (see Duvvuru, page 174, right column). If the BTAC does not contain the target address of a branch, the target address is computed later in the pipeline and BTAC is updated (see Duvvuru, page 174, right column). Accordingly, Duvvuru teaches that the branch target address is previously stored in BTAC or computed later in the pipeline. As such, Duvvuru fails to explicitly teach or suggest computing a conditional jump address prior to receipt of I/O read data, as claimed.

Moreover, Duvvuru discloses the impact of register relative branches such that the register relative branch instruction is emitted to implement a branch where the target is dynamically set, and where the branch target address is either computed on the fly or loaded from memory (see Duvvuru, page 176, right column). Accordingly, in register relative branching Duvvuru teaches computing the branch target address on the fly or loading it from memory. Therefore, Duvvuru fails to explicitly teach or suggest computing a conditional jump instruction address prior to receipt of I/O read data, as claimed.

Furthermore, Duvvuru discloses that if the target address in the BTAC is hit, the target address and associated cc bit number are read out (see Duvvuru, page 174, right column). The Applicant respectfully submits that reading out target address and associated cc bit number as disclosed by Duvvuru differs from determining whether to execute at a next consecutive address or at the conditional jump address, as claimed.

Moreover, even though the rejection admits that Fleisher and Grunert fails to teach a virtual microcontroller computing a conditional jump address to remain in lockstep execution with the microcontroller, as claimed, the rejection fails to address this limitation. The Applicant respectfully reminds the Examiner that to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all the claim limitations (see MPEP 2100-126). Furthermore, the Applicant does not understand Duvvuru to teach or suggest that a virtual microcontroller computes a conditional jump address to remain in lockstep execution with the microcontroller, as claimed. Therefore, the rejection fails to establish a prima facie case of obviousness, under 35 U.S.C. §103(a)

Accordingly, the Fleisher alone or in combination with Grunert and Duvvuru fails to render independent Claim 1 obvious, under 35 U.S.C. §103(a). Independent Claims 6 and 14 are similar in scope to that of independent Claim 1

and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

Claims 3 and 4 are rejected, under 35 U.S.C. §103(a), as being allegedly unpatentable over Fleisher in view of Grunert and in view of Duvvuru as applied to Claim 1, and further in view of Official Notice. The Applicant respectfully traverses in view of the following.

The Applicant respectfully reminds the Examiner that it is improper to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based (see MPEP §2144.03(A) and see *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697). Moreover, the Applicant respectfully reminds the Examiner that the rejection must point to some concrete evidence in the record in support of these findings to satisfy the substantial evidence test (see MPEP 2144.03(c)). Moreover, the Applicant respectfully reminds the Examiner that if the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding (see 37 CFR 1.104(d)(2) and see MPEP 2100-144).

Claims 10 and 11 recite limitations similar to that of Claims 3 and 4 and are therefore patentable for similar rationale. Accordingly, allowance of Claims 3-4 and 10-11 is earnestly solicited.

As per Claims 7 and 8, the rejection states that Claims 7 and 8 recite a method employed by the system of Claims 1 and 3-5. The Applicant respectfully traverses in view of the following. Claims 7 and 8 are patentable by virtue of their dependency. Moreover, as discussed above Duvvuru fails to teach or suggest determining whether to execute at a next consecutive address or at the conditional jump address, as claimed. For similar rationale, Duvvuru fails to teach or suggest executing a next consecutive instruction in the event the conditional jump condition is not met, as claimed. Similarly, Duvvuru fails to teach or suggest executing an instruction at the conditional jump address in the event the conditional jump condition is met, as claimed. Accordingly, allowance of Claims 7 and 8 is earnestly solicited.

Claims 14-16 and 18-20 recite limitations similar to that of Claims 6-8 ad 10-12 and are therefore patentable for similar reasons. As such, allowance of Claims 14-16 and 18-20 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of these rejections under 35 U.S.C. §101, 35 U.S.C. §112 and 35 U.S.C. §103.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-20 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-20 overcome the rejections of record and, therefore, allowance of Claims 1-20 is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,
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